REMARKS/ARGUMENTS

Claims 1-3, 6, and 7 stand rejected under 35 U.S.C. 102(e) as being anticipated by Lahaug; claims 4, 5, and 8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lahaug as applied to claims 1-3, 6, and 7, and further in view of Chau.

Claim 1 comprises the limitations of forming a first dielectric layer on said semiconductor substrate; performing a first plasma nitridation of said first dielectric layer; removing said first dielectric from a region of said substrate; forming a second dielectric layer on said semiconductor substrate in said region from which said first dielectric layer were removed; and simultaneously performing a second plasma nitridation of said second dielectric layer and said first dielectric layer.

The Lahaug reference describes a process consisting of forming a first dielectric layer, forming an oxynitride layer on said dielectric layer, removing a region of the dielectric layer, and forming a second dielectric layer of silicon oxide. Contrary to the examiner's assertions, the Lahaug reference does not describe simultaneously performing a second plasma nitridation of the second dielectric layer as claimed in claim 1. For a 35 U.S.C. 102 rejection to be valid, each and every element of the claimed invention must be described in the cited reference. The claimed limitation of simultaneously performing a second plasma nitridation of said second dielectric layer and said first dielectric layer is not found in the cited reference and claim 1 is allowable over the cited reference. It should be noted that the composition of a transistor dielectric is a very exacting and depends on the type of transistor. It is therefore not obvious that a second plasma nitridation process can be applied to the dielectric layers described in the Lahaug reference. A second plasma nitridation process applied to the dielectric layers in the Lahaug reference would render the resulting dielectric layers totally unsuitable for the application described in the reference.

Claim 6 comprises the limitations of providing a semiconductor substrate; forming a first silicon oxide layer; performing a plasma nitridation process on said first silicon oxide layer forming a first plasma nitrided oxide layer; removing said first plasma nitrided oxide layer from regions of said substrate; and forming a second plasma nitrided oxide layer on said semiconductor substrate in said regions from which said first plasma nitrided oxide layer was removed. As described above, the Lahaug reference does not describe the formation of a second plasma nitrided oxide layer on said semiconductor substrate in said regions from which said first plasma nitrided oxide layer was removed and as such claim 6 is also allowable over the cited art.

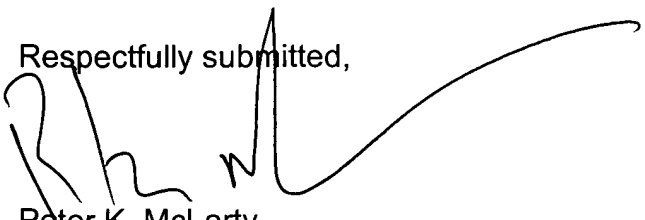
Claims 2-5 and 7-8 depend on claims 1 and 6 respectively and therefore contain all the limitations of these claims. Claims 2-5 and 7-8 are therefore also allowable over the Lahaug reference either singly or in combination with the Chau et al. reference.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



Peter K. McLarty
Attorney for Applicants
Reg. No. 44,923

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-4258

Amendments to the Drawings:

None